

SMARTMESH IA-510™ M2510

2.4 GHz Wireless Mote

Product Description

The WirelessHART™-compliant M2510 combines Dust Networks' robust Intelligent Networking Platform and industry-leading low-power radio technology in an easy-to-integrate 22-pin module. As part of the SmartMesh IA-510™ system, the M2510 provides industrial automation vendors with an embedded wireless system complete with modular radio certifications for easy integration and reuse in developing multiple WirelessHART products.

The M2510 is tailored for use in battery-powered and energy-scavenging wireless devices, and is engineered for applications that demand proven performance and scalability. With Dust Networks' innovative IEEE 802.15.4-compliant design and integrated power amplifier, the M2510 enables a decade of battery life on two AA batteries. Additionally, all motes can function as both battery-powered routers and nodes, enabling a full mesh topology that provides more redundant routes and higher network performance.

The network-ready module integrates all radio circuitry components, including an MMCX-type antenna connector, to eliminate the burden of complex RF design. The international modular certifications, fully engineered RF solution, comprehensive APIs and Development Support Suite of the M2510 mote module offer rapid field device integration, and reduced development time and cost for WirelessHART solutions.

About SmartMesh IA-510

Dust Networks' SmartMesh IA-510 is the first WirelessHART-compatible system in the SmartMesh IA-500™ family of products. The SmartMesh IA-510 system offers industrial automation vendors an industry-leading standards-based system that delivers flexible, secure solutions. The SmartMesh IA-510 system's Intelligent Networking Platform delivers dynamic network optimization and intelligent routing to achieve the carrier-class data reliability, lower latency, and deterministic power management required for the industrial automation market. The SmartMesh IA-510 system consists of the PM2510 embedded network manager and two mote form factors: the DN2510 Mote-on-Chip™ and the M2510 RF-certified mote module. SmartMesh IA-510 systems are easy for industrial automation vendors to integrate and simple for end users to deploy.

Key Features

Wireless HART Compliance

- Interoperable with other WirelessHART field devices and gateways

Superior Reliability

- >99.99% data reliability even in the most challenging industrial environments
- Every M2510 can act as both an endpoint and a router, increasing network reliability
- Leverages SmartMesh IA-510's network manager's Intelligent Networking Platform to ensure optimal mote performance

Easy Integration

- Fully engineered RF—power amplifier, balun, crystals, antenna matching circuitry and antenna connector on module
- Comprehensive APIs deliver rich functionality and flexibility without complex coding

Ultra-low Power Consumption

- Industry-leading radio technology optimized for battery-powered operation
- Over a decade of network operation on two AA batteries
- Automatic network-wide coordination for efficient power usage

Global Market Solution

- Modular RF certifications pending for FCC, IC, and CE
- IEEE 802.15.4-certified radio operates on 2.4 GHz global license-free band
- Configurable radio output power—meets RF emission limits for different regions with a single product

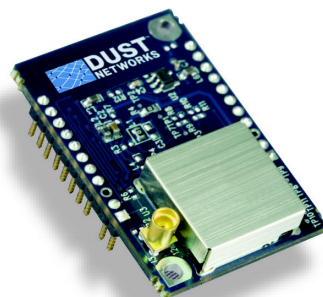
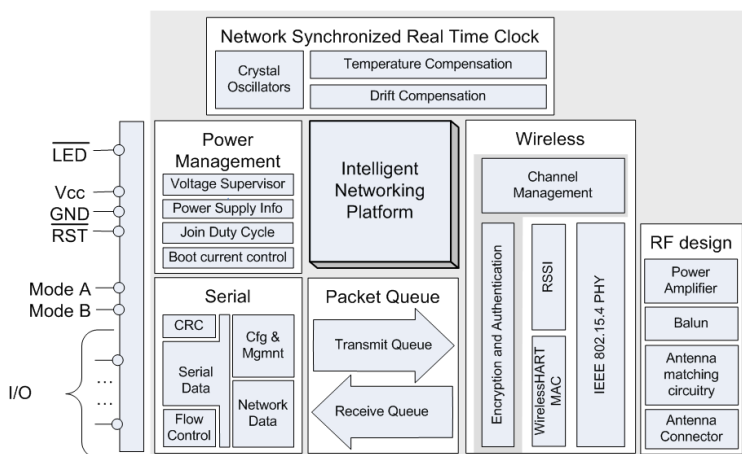


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1.0 Absolute Maximum Ratings

The absolute maximum ratings shown below should not be violated under any circumstances. Permanent damage to the device may be caused by exceeding one or more of these parameters.

Unless otherwise noted, all voltages in Table 1 are made relative to V_{SS} .

Table 1 Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units	Comments
Supply voltage (V_{DD} to V_{SS})	-0.3		3.6	V	
Voltage on any digital I/O pin	-0.3		$V_{DD} + 0.3$ up to 3.6	V	
Input RF level			10	dBm	Input power at antenna connector
Storage temperature range	-40		+85	°C	
Lead temperature			+260	°C	For 10 seconds
VSWR of antenna			3:1		
ESD protection					
Antenna pad			±250	V	HBM
All other pads			±2	kV	HBM
			±200	V	CDM



Caution! ESD sensitive device. Precaution should be used when handling the device to prevent permanent damage.

2.0 Normal Operating Conditions

Unless otherwise noted, Table 2 assumes V_{DD} is 3.0 V and temperature is 25 °C.

Table 2 Normal Operating Conditions

Parameter	Min	Typ	Max	Units	Comments
Operational supply voltage range (between V_{DD} and V_{SS})	2.75		3.3	V	Including noise and load regulation
Voltage supply noise			250	mV _{p-p}	50 Hz to 2 MHz
Voltage supervisor trip point		2.64		V	Reset trip point
Peak current					
			85	mA	Flash write 35 ms max
			6	mA	Searching for network, typically 30 ms on and 570 ms in sleep for up to 60 minutes
			12	mA	Mote boot, see section 6.2
Power amplifier enabled			18	mA	TX, 5 ms maximum
Power amplifier disabled			7	mA	TX, 5 ms maximum
			TBD	mA	\overline{RST} asserted
Operating temperatures	-40		+85	°C	
Maximum allowed temperature ramp during operation			8	°C/min	-40 °C to +85 °C
Operating relative humidity	10		90	% RH	Non-condensing

Unless otherwise noted, Table 3 assumes V_{DD} is 3.0 V.

Table 3 Current Consumption

Parameter	Min	Typ	Max	Units	Comments
Transmit					
Power amplifier enabled		18		mA	
Power amplifier disabled		7		mA	
Receive		6		mA	
Sleep		3		μ A	

3.0 Electrical Specifications

Table 4 Device Load

Parameter	Min	Typ	Max	Units	Comments
Total capacitance			6	μ F	V_{DD} to V_{SS}
Total inductance			4.9	μ H	

Unless otherwise noted, V_{DD} is 3.0 V and temperature is -40°C to $+85^{\circ}\text{C}$.

Table 5 Digital I/O Type 1

Digital Signal	Min	Typ	Max	Units	Comments
V_{IL} (low-level input voltage)	-0.3		0.6	V	
V_{IH} (high-level input voltage)	$0.8 \times V_{DD}$		$V_{DD} + 0.3$	V	
V_{OL} (low-level output voltage)			0.4	V	
V_{OH} (high-level output voltage)	2.4			V	
Digital current*					
Output source (single pin)		3.7		mA	25°C
Output sink (single pin)		2.0		mA	25°C
Input leakage current		50		nA	25°C

* This current level guarantees that the output voltage meets V_{OH} and V_{OL} specifications above.

Table 6 Digital I/O Type 2

Digital Signal	Min	Typ	Max	Units	Comments
V_{IL} (low-level input voltage)	-0.3		0.6	V	
V_{IH} (high-level input voltage)	$0.8 \times V_{DD}$		$V_{DD} + 0.3$	V	
V_{OL} (low-level output voltage, multi-function I/O configured as output)	-0.3		0.6	V	$I_{OL} < 0.6 \text{ mA}$, 85°C
V_{OH} low-level output voltage, multi-function I/O configured as output)	$V_{DD} - 0.6$		V_{DD}	V	$I_{OH} > -0.6 \text{ mA}$, 85°C
Digital current*					
Output source (single pin, multifunction I/O configured as output)		0.4		mA	25°C
Output sink (single pin, multifunction I/O configured as output)		0.6		mA	25°C
Input leakage current		50		nA	25°C

Digital Signal	Min	Typ	Max	Units	Comments
* This current level guarantees that the output voltage meets V_{OH} and V_{OL} specifications above.					

Table 7 Digital I/O Type 3

Digital Signal	Min	Typ	Max	Units	Comments
V_{IL} (low-level input voltage)	-0.3		0.6	V	
V_{IH} (high-level input voltage)	2.0		$V_{DD} + 0.3$	V	
V_{OL} (low-level output voltage)			0.4	V	
V_{OH} (high-level output voltage)	$V_{DD} - 0.2$			V	
Digital current*					
Output source (single pin)		100		μA	25 °C
Output sink (single pin)		1.6		mA	25 °C
Input leakage current		50		nA	25 °C
* This current level guarantees that the output voltage meets V_{OH} and V_{OL} specifications above.					

4.0 Radio

4.1 Detailed Radio Specifications

Table 8 Detailed Radio Specifications

Parameter	Min	Typ	Max	Units	Comments
Operating frequency	2.4000		2.4835	GHz	
Number of channels		15			
Channel separation		5		MHz	
Occupied channel bandwidth		2.7		MHz	At -20 dBc
Frequency Accuracy	-40		+40	ppm	
Modulation					IEEE 802.15.4 DSSS
Raw data rate		250		kbps	
Receiver operating maximum input level		0		dBm	
Receiver sensitivity		-92.5		dBm	At 50% PER, $V_{DD} = 3 V$, 25 °C
		-90		dBm	At 1% PER, $V_{DD} = 3 V$, 25 °C
Output power, conducted					
Power amplifier enabled		+8		dBm	$V_{DD} = 3 V$, 25 °C
Power amplifier disabled		-2		dBm	$V_{DD} = 3 V$, 25 °C

Parameter	Min	Typ	Max	Units	Comments
Range*					
Power amplifier enabled:					
Indoor		100		m	
Outdoor		300		m	25 °C, 50% RH, 1 meter above ground, +2 dBi omni-directional antenna
Power amplifier disabled:					
Indoor		25		m	
Outdoor		200		m	25 °C, 50% RH, 1 meter above ground, +2 dBi omni-directional antenna
* Actual RF range performance is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, actual performance varies for each instance.					

4.2 Antenna Specifications

A MMCX-compatible male connector is provided on board for the antenna connection. The antenna must meet specifications in Table 9. For a list of FCC-approved antennae see section 9.1.2.

Table 9 Antenna Specifications

Parameter	Value
Frequency range	2.4 – 2.4835 GHz
Impedance	50 Ω
Maximum VSWR	3:1
Connector	MMCX*
* The M2510 can accommodate the following RF mating connectors: <ul style="list-style-type: none"> • MMCX straight connector such as Johnson 135-3402-001, or equivalent • MMCX right angle connector such as Tyco 1408149-1, or equivalent 	

When the mote is placed inside an enclosure, the antenna should be mounted such that the radiating portion of the antenna protrudes from the enclosure. The antenna should be connected using a MMCX connector on a coaxial cable. For optimum performance, the antenna should be positioned vertically when installed.

5.0 Pinout

The M2510 has two 11-pin Samtec MTMM-111-04-S-S-175-3 (or equivalent) connectors on the bottom side for handling all of the I/O. The third pin in each of the connectors is not populated, and serves as a key for alignment. The connectors are mounted on opposite edges of the long axis of the M2510.

5.1 M2510 Pinout

The M2510 provides a bidirectional flow-controlled serial interface (see section 7.5 Settable I/O Modes).

Table 10 M2510 Pin Functions

Pin Number	Pin Name	Description	I/O Type	Direction
1	V _{SS}	Ground	Power	–
2	V _{DD}	Power	Power	–
3	KEY (no pin)	–	–	–
4	RX	UART Rx	2	In
5	TX	UART Tx	2	Out
6	$\overline{\text{LED}}$	Active low led turn on	1	Out
7	$\overline{\text{MT_RTS}}$	UART active low mote ready to send	2	Out
8	$\overline{\text{MT_CTS}}$	UART active low mote clear to send	1	Out
9	$\overline{\text{SP_CTS}}$	UART active low serial peripheral clear to send	2	In
10	$\overline{\text{TIME}}$	Falling edge time request	2	In
11	Mode_pin_B	Selects between Mode 1 & Mode 3 operation	2	In
12	$\overline{\text{FLASH_P_EN}}$	Active low flash power enable	1	In*
13	<i>Reserved</i>	Do not connect	–	–
14	<i>Reserved</i>	Do not connect	–	–
15	<i>Reserved</i>	Do not connect	–	–
16	<i>Reserved</i>	Do not connect	–	–
17	SCK	SPI clock	3	In*
18	MOSI	SPI master out slave in serial data	3	In*
19	MISO	SPI master in slave out serial data	3	Out*
20	KEY (no pin)	–	–	–
21	$\overline{\text{SPI_CS}}$	Active low flash chip select	3	In*
22	$\overline{\text{RST}}$	Active low reset	1	In

* The direction associated with the flash interface are defined when the device is held in reset and is intended solely for the use of in circuit programming of the device. Following reset all inputs will become outputs and must not be driven externally.

The $\overline{\text{RST}}$ input pin is internally pulled up, and connecting it is optional. When driven active low, the mote is hardware reset until the signal is de-asserted. Refer to section 6.1 for timing requirements on the $\overline{\text{RST}}$ pin. Note that the mote may also be reset using the mote serial command (see the *SmartMesh IA-510 Mote Serial API Guide*).

The $\overline{\text{TIME}}$ input pin is optional, and must either be driven or pulled up with a 5.1 M Ω resistor. Unless noted otherwise, all signals are active low.

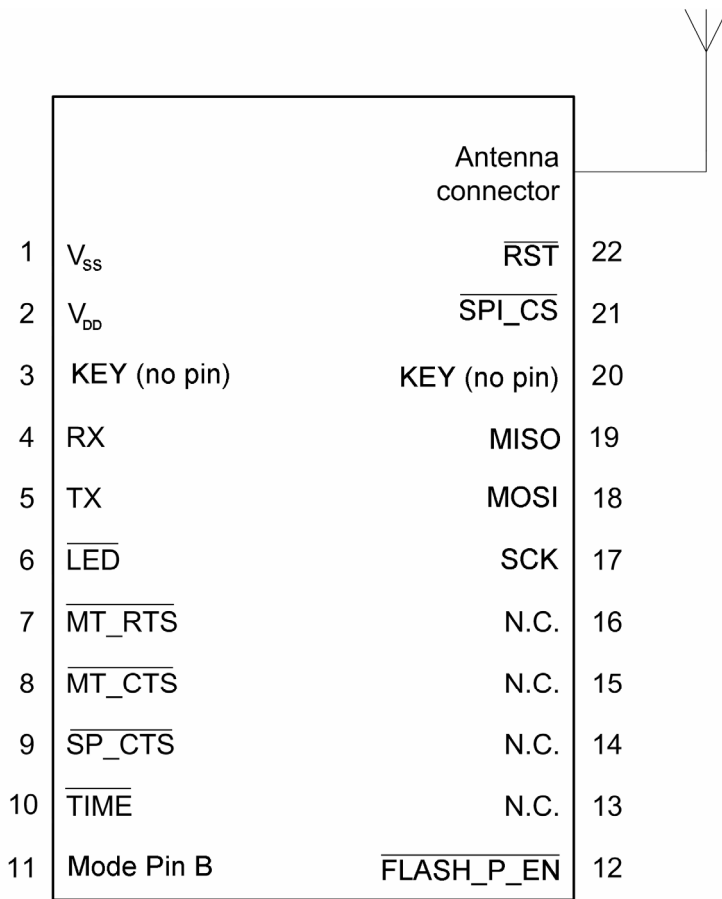


Figure 1 M2510 Package with Pin Labels

6.0 Mote Boot Up

6.1 Power-on Sequence

The M2510 has internal power-on reset circuits that ensure that the mote will properly boot. However, for the power-on reset circuitry to function properly the external power supply must meet the timing shown in Figure 2 and specified in Table 11.

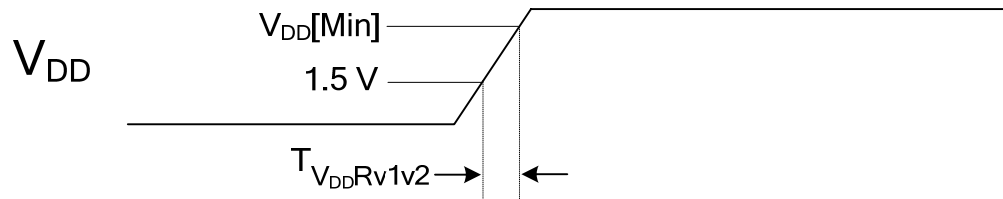


Figure 2 External Power Supply Timing Requirement

The following reset sequence (shown in Figure 3 and specified in Table 11) is required for external power supplies that fail to meet the requirement above.

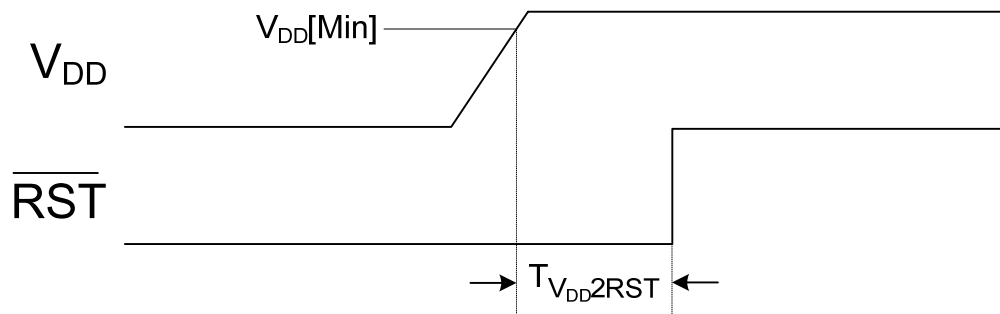


Figure 3 Power-on Sequence

Table 11 Power-on Sequence

Parameter	Min	Typ	Max	Units	Comments
TV_{DD2RST}	125			μs	
$TV_{DDRV1v2}$			1	ms	
\overline{RST} pulse width	125			μs	Reset timing

6.2 Inrush Current

During power on, the mote can be modeled as a lumped impedance, as shown in **Error! Reference source not found.** . With a source impedance (R_{src}) of $1\ \Omega$, the inrush current on the mote appears as shown in **Error! Reference source not found.**.

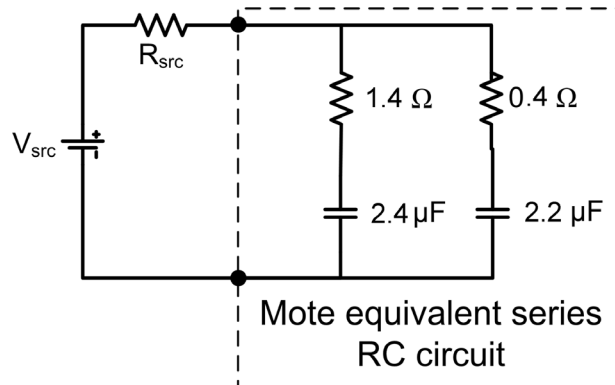
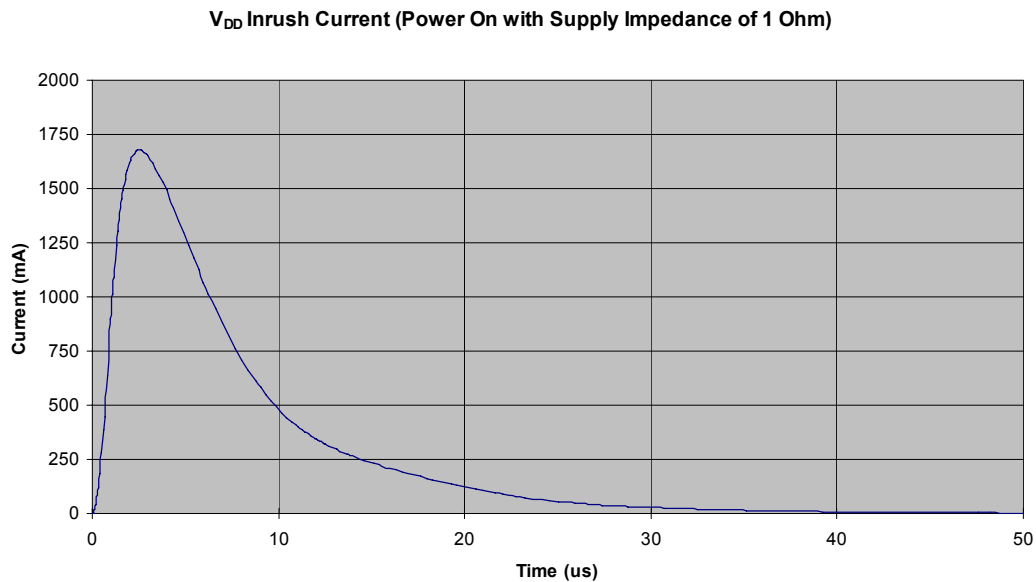


Figure 4 M2510 Equivalent Series RC Circuit

Figure 5 V_{DD} Inrush Current

6.3 Mote Boot Sequence

Following the negation of \overline{RST} the mote completes its boot up process by loading and decrypting the application image and loading the operating parameters. During the boot process, the mote's output signals are not actively driven and the input signals are ignored.

The DN2510 supports two mote boot modes: standard boot and low current boot. Standard boot is optimized for quick boot time. Low current boot lowers the average current but at a longer boot time. The mote boot mode is determined by the software executable loaded onto the DN2510.

6.3.1 Standard Boot

When the DN2510 operates in standard boot, the time between the mote power up and the serial interface availability is defined as t_{boot_delay} and specified in Table 12 Standard Boot Sequence below. The peak current during mote boot is specified under Peak Current in **Error! Reference source not found.**

Table 12 Standard Boot Sequence

Parameter	Min	Typ	Max	Units	Comments
t_{boot_delay}			6	s	The time between mote power up and serial interface availability.

6.3.2 Low Current Boot

When operating in Low Current Boot, the DN2510 lowers average current consumption by spreading the boot operation over a longer time. This mode is intended to support systems with supplies having a maximum DC current less than the peak current required by the DN2510. These systems must store enough charge to maintain the supply through the DN2510's peak current consumption. The peak “average current” consumption for the M2510 is defined by the maximum total charge Q consumed over a sliding window in time, T_{window} .

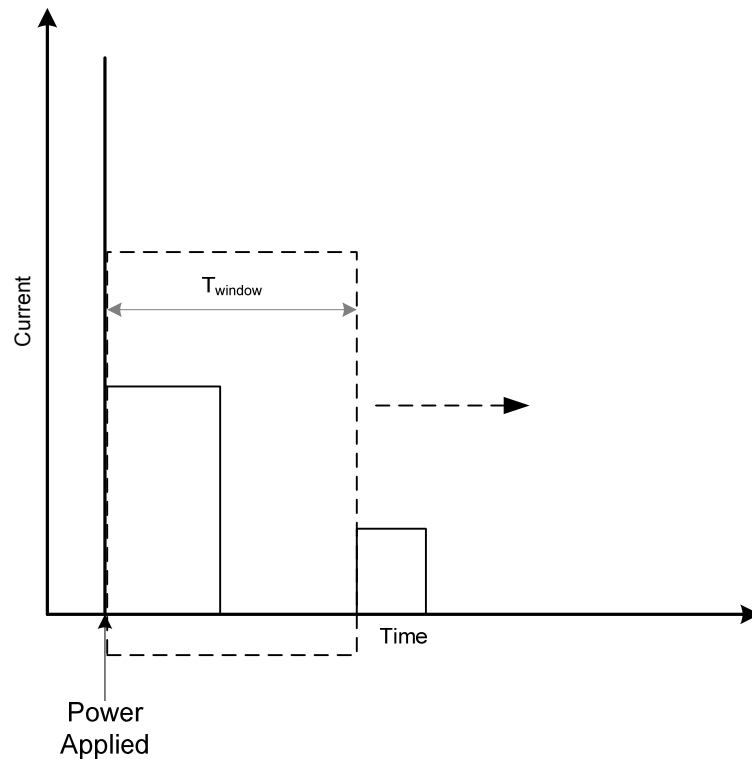


Figure 6 Low Current Boot Sequence

Table 13 Low Current Boot Sequence

Parameter	Min	Typ	Max	Units	Comments
t_{boot_delay}			TBD	s	The time between mote power up and serial interface availability.
T_{window}			TBD	ms	
Q			2.5	mC	

6.4 Serial Interface Boot Up

6.4.1 M2510 Serial Interface Boot Up

Upon M2510 power up, the $\overline{MT_CTS}$ line is high (inactive). The M2510 serial interface boots within t_{boot_delay} (see 6.2 **Error! Reference source not found.**) of the mote powering up, at which time the M2510 will transmit an HDLC boot event packet. Note that full handshake is in effect and is required to receive this packet.

7.0 Interfaces

7.1 Reset Pin

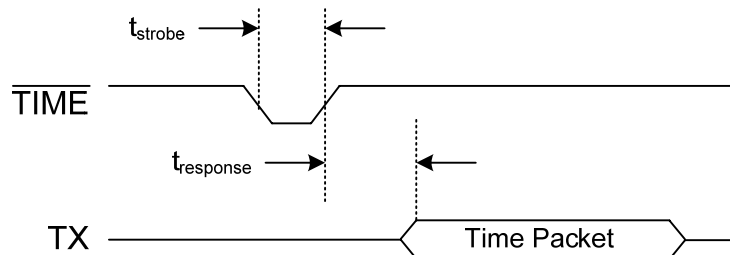
The \overline{RST} input pin is internally pulled up. Connecting it is optional; however, in applications operating in the presence of EMI, \overline{RST} should be actively driven high. When driven low, the mote hardware is in reset. Note that the mote may also be reset using the mote serial command 0x8D Reset Mote. For requirements on reset timing, see section 6.1. If a system is designed to assert \overline{RST} after the mote has completed its boot process, it is recommended that the mote be placed into deep sleep using the 0x09 lowPowerSleep command prior to assertion of the \overline{RST} signal. For detailed information about mote serial commands, refer to the *SmartMesh IA-510 Mote Serial API Guide*.

7.2 Timestamps

The M2510 has the ability to deliver network-wide synchronized timestamps. The M2510 sends a time packet (as described in the *SmartMesh IA-510 Mote Serial API Guide*) through its serial interface when one of the following occurs:

- Mote receives an HDLC request to read time
- The \overline{TIME} signal is asserted

The \overline{TIME} pin is optional and has the advantage of being more accurate. The value of the timestamp is taken within approximately 1 ms of receiving a \overline{TIME} signal activation. If the HDLC request is used, due to packet processing the value of the timestamp may be captured several milliseconds after receipt of the packet. The real time delivered to the sensor processor is relative to the real time clock on the Manager, which serves as the Network Real Time Clock (NRTC). The time stamp skew across the network is guaranteed to be within ± 250 ms of the NRTC.

Figure 7 Operation of \overline{TIME} PinTable 14 \overline{TIME} Timing Values

Variable	Description	Min	Max	Units
t_{strobe}	\overline{TIME} strobe pulse width	125		μs
$t_{response}$	Negation of Time strobe to start of time packet		100	ms

7.3 Status $\overline{\text{LED}}$ Signal

The M2510 provides an output that can be used to drive a status LED. This signal indicates network connectivity information, which is most useful during mote installation. Alternatively, the mote's network status may be polled via serial using the Get Parameter request with the mote state parameter (for details see the *SmartMesh IA-510 Mote Serial API Guide*).

Table 15 Status $\overline{\text{LED}}$ Signal

LED Signal Behavior	Mote State
High	Off, or in sleep mode
Single blink (750 ms low, 3 s high)	On, and searching for potential network
Double blink (750 ms low, 750 ms high, 750 ms low, 3 s high)	On, and attempting to join the network
Triple blink (750 ms low, 750 ms high, 750 ms low, 750 ms high, 750 ms low, 3 s high)	On, and attempting to establish redundant links
Low	On, fully configured into network with redundant parents

7.4 SPI Mote Programming Interface

The M2510 features a Serial Peripheral Interface (SPI) for programming the mote software during the OEM manufacturing process. With this mote programming capability, OEMs may exercise revision control of the mote software in their final product.

OEM designs must include a connection to the SPI pins ($\overline{\text{FLASH_P_EN}}$, $\overline{\text{SPI_CS}}$, SCK, MOSI, MISO, $\overline{\text{RST}}$, V_{SS}) suitable for their needs. Please refer to *DN2510, M2510 Integration Guide* for detailed layout and SPI programmer recommendations.

7.5 Settable I/O Modes

The M2510 offers a choice of two I/O modes. The functionality of the interface will be determined by the setting of Mode pin B whose pinout is described in 5.0 Pinout.

Table 16 Mode Pin Settings

Pin	Mode 1	Mode 3
Mode pin B	Externally tied low	Externally tied high

All modes provide a means of transmitting and receiving serial data through the wireless network, as well as a command interface that provides synchronized time stamping, local configuration, and diagnostics.

Mode 1 implements an 8-bit, no parity, 9600 bps baud three, four or five-signal serial interface with bidirectional packet-level flow control operating at 9600 bps. In certain OEM designs, one or two of the serial handshake signals may be optional for reduced pin count, as described in Table 17.

Mode 3 implements an 8-bit, no parity, 115.2 kbps baud five-signal serial interface with bidirectional packet-level flow control and byte-level flow control in the mote-to-microprocessor direction only.

7.5.1 Mode 1: Three/Four/Five-signal Serial Interface (9600 bps)

The M2510 mode 1 provides a three, four, or five-signal serial interface that is optimized for low-powered embedded applications (and in certain designs may provide a low pin count serial solution). The mode 1 serial interface is comprised of the data pins (TX, RX) as well as handshake pins ($\overline{\text{MT_RTS}}$, $\overline{\text{MT_CTS}}$, $\overline{\text{SP_CTS}}$) used for bidirectional flow control. The $\overline{\text{MT_RTS}}$ signal is ideal for designs where the microprocessor requires extra time to prepare to receive a packet (for example, the OEM microprocessor sleeps periodically, but requires a wake-up signal prior to receiving a packet). Refer to Table 17 for information on each handshake pin, including details on which pins are optional.

Table 17 Mode 1 Pin Usage

Pin	I/O	Usage
RX	Input	Serial data moving from the microprocessor to the mote.
TX	Output	Serial data moving from the mote to the microprocessor.
$\overline{\text{MT_RTS}}$	Output	<p>$\overline{\text{MT_RTS}}$ provides a mechanism to wake up the microprocessor in order to receive a packet. This signal is asserted when the mote is ready to send a serial packet. The signal stays low until the $\overline{\text{SP_CTS}}$ signal from the microprocessor is detected low by the mote (indicating readiness to receive a packet) or the $t_{\text{MT_RTS to SP_CTS}}$ timeout defined in Section 7.5.3 expires.</p> <p>$\overline{\text{MT_RTS}}$ may be ignored by the microprocessor only if $\overline{\text{SP_CTS}}$ always stays low.</p>
$\overline{\text{SP_CTS}}$	Input	<p>$\overline{\text{SP_CTS}}$ provides packet-level flow control for packets transferred from the mote to the microprocessor. When the microprocessor is capable of receiving a packet it should assert the $\overline{\text{SP_CTS}}$ signal.</p> <p>$\overline{\text{SP_CTS}}$ may be externally tied low (reducing pin count) only if the microprocessor is always ready to receive a serial packet.</p>
$\overline{\text{MT_CTS}}$	Output	<p>$\overline{\text{MT_CTS}}$ provides packet-level flow control for packets transferred from the microprocessor to the mote that are destined for transfer over the network. Upon reset, following boot the mote will negate $\overline{\text{MT_CTS}}$ until the mote establishes a wireless network connection. During operation, the mote will negate $\overline{\text{MT_CTS}}$ if the mote does not have sufficient buffering to accept another packet. $\overline{\text{MT_CTS}}$ will also remain high if the mote is not part of the network. The microprocessor must check that the $\overline{\text{MT_CTS}}$ pin is low before initiating each serial packet for wireless transmission.</p> <p>Note that the mote may receive local serial packets at any time regardless of the $\overline{\text{MT_CTS}}$ state. (For a list of local commands, see the <i>SmartMesh IA-510 Mote Serial API Guide</i>.)</p>
$\overline{\text{TIME}}$	Input	The $\overline{\text{TIME}}$ pin can be used for triggering a timestamp packet. Its usage is optional.

7.5.2 Mode 3: Five-signal Serial Interface (115.2 kbps)

The M2510 mode 3 provides a five-signal serial interface with byte-level flow control on transfers from the mote to the microprocessor. The mode 3 serial interface is comprised of the data pins (TX, RX) as well as handshake pins ($\overline{\text{MT_RTS}}$, $\overline{\text{MT_CTS}}$, $\overline{\text{SP_CTS}}$) used for bidirectional flow control. The $\overline{\text{MT_RTS}}$ signal is ideal for designs where the microprocessor requires extra time to prepare to receive a packet (for example, the OEM microprocessor sleeps periodically, but requires a wake-up signal prior to receiving a packet). In order to support 115.2 kbps the microprocessor must include two framing bytes, 0x7E, at the start of each packet sent from the microprocessor to the mote. Refer to Table 18 for information on each handshake pin, including details on which pins are optional.

Table 18 Mode 3 Pin Usage

Pin	I/O	Usage
RX	Input	Serial data moving from the microprocessor to the mote.
TX	Output	Serial data moving from the mote to the microprocessor.
$\overline{\text{MT_RTS}}$	Output	$\overline{\text{MT_RTS}}$ provides a mechanism to wake up the microprocessor in order to receive a packet. This signal is asserted when the mote is ready to send a serial packet. The signal stays low until the $\overline{\text{SP_CTS}}$ signal from the microprocessor is detected low by the mote (indicating readiness to receive a packet) or the $t_{\overline{\text{MT_RTS}} \text{ to } \overline{\text{SP_CTS}}}$ timeout defined in Section 7.5.3 expires.
$\overline{\text{SP_CTS}}$	Input	$\overline{\text{SP_CTS}}$ provides both packet-level and byte-level flow control for packets transferred from the mote to the microprocessor. When the microprocessor is capable of receiving a packet it should assert the $\overline{\text{SP_CTS}}$ signal. In mode 3 byte-level flow control is achieved by having the microprocessor negate and then reassert the $\overline{\text{SP_CTS}}$ signal following the receipt of each byte. The mote will begin transmission of the next byte after detecting the reassertion of $\overline{\text{SP_CTS}}$.
$\overline{\text{MT_CTS}}$	Output	$\overline{\text{MT_CTS}}$ provides packet-level flow control for packets transferred from the microprocessor to the mote that are destined for transfer over the network. Upon reset, following boot the mote will negate $\overline{\text{MT_CTS}}$ until the mote establishes a wireless network connection. During operation, the mote will negate $\overline{\text{MT_CTS}}$ if the mote does not have sufficient buffering to accept another packet. $\overline{\text{MT_CTS}}$ will also remain high if the mote is not part of the network. The microprocessor must check that the $\overline{\text{MT_CTS}}$ pin is low before initiating each serial packet for wireless transmission. Note that the mote may receive local serial packets at any time regardless of the $\overline{\text{MT_CTS}}$ state. (For a list of local commands, see the <i>SmartMesh IA-510 Mote Serial API Guide</i> .)
$\overline{\text{TIME}}$	Input	The $\overline{\text{TIME}}$ pin can be used for triggering a timestamp packet. Its usage is optional.

7.5.3 UART AC Timing

Table 19 UART Timing Values

Variable	Description	Min	Max	Units
$t_{\text{RX_BAUD}}$	Deviation from baud rate	-2	+2	%
$t_{\text{RX_STOP}}$	Number of stop bits (9600 bps)	1		bit period
$t_{\text{RX_STOP}}$	Number of stop bits (115.2 kbps)	1.5		bit period
$t_{\text{TX_BAUD}}$	Deviation from baud rate	-1	+1	%
$t_{\text{TX_STOP}}$	Number of stop bits	1		bit period
$t_{\overline{\text{SP_CTS}} \text{ to } \overline{\text{MT_RTS}}}$	Assertion of $\overline{\text{SP_CTS}}$ to negation of $\overline{\text{MT_RTS}}$	0	10	ms
$t_{\overline{\text{MT_RTS}} \text{ to } \overline{\text{SP_CTS}}}$	Assertion of $\overline{\text{MT_RTS}}$ to assertion of $\overline{\text{SP_CTS}}$		500	ms
$t_{\overline{\text{SP_CTS}} \text{ to TX}}$	Assertion of $\overline{\text{SP_CTS}}$ to start of byte	0	10	ms
$t_{\text{TX to } \overline{\text{SP_CTS}}}$	Start of byte to negation of $\overline{\text{SP_CTS}}$	1		bit period
$t_{\overline{\text{SP_CTS}} \text{ ack PW}}$	Negation pulse width of $\overline{\text{SP_CTS}}$	500		ns
$t_{\text{interbyte_timeout}}$	Falling edge of TX to falling edge of $\overline{\text{SP_CTS}}$ (Mode 3 only)		7.1	ms

Variable	Description	Min	Max	Units
$t_{\text{interpacket_delay}}$	The sender of an HDLC packet must wait at least this amount of time before sending another packet	20		ms

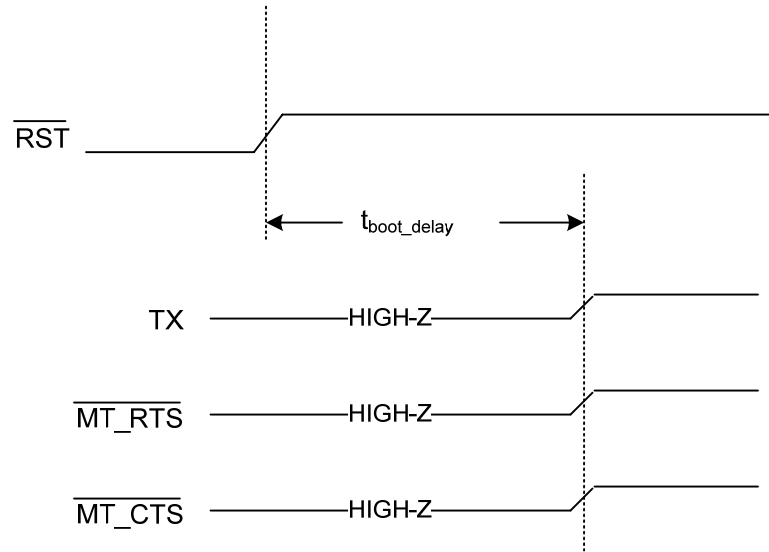


Figure 8 Power-on Sequence (see 6.2 “Inrush Current

Figure 9 During power on, the mote can be modeled as a lumped impedance, as shown in Error! Reference source not found. . With a source impedance (R_{src}) of $1\ \Omega$, the inrush current on the mote appears as shown in Error! Reference source not found..

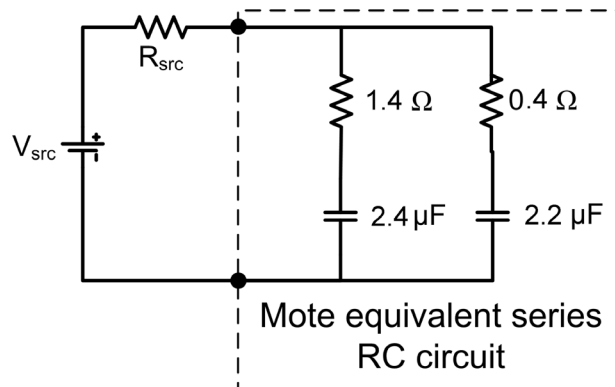


Figure 10 M2510 Equivalent Series RC Circuit

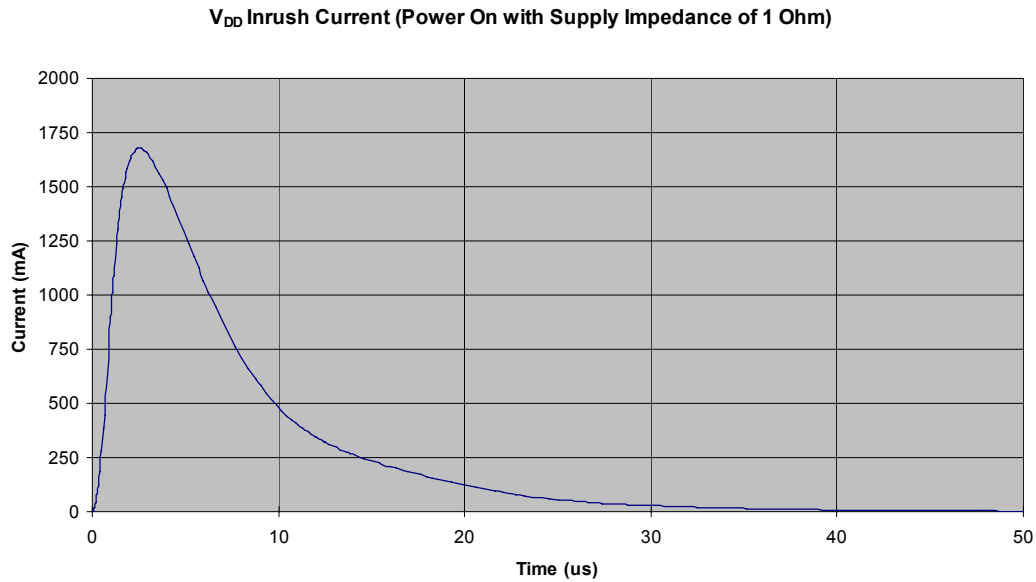


Figure 11 VDD Inrush Current

7.6 Mote Boot Sequence

Following the negation of the mote completes its boot up process by loading and decrypting the application image and loading the operating parameters. During the boot process, the mote's output signals are not actively driven and the input signals are ignored.

The DN2510 supports two mote boot modes: standard boot and low current boot. Standard boot is optimized for quick boot time. Low current boot lowers the average current but at a longer boot time. The mote boot mode is determined by the software executable loaded onto the DN2510.

7.6.1 Standard Boot

When the DN2510 operates in standard boot, the time between the mote power up and the serial interface availability is defined as `tboot_delay` and specified in Table 12 Standard Boot Sequence below. The peak current during mote boot is specified under Peak Current in **Error! Reference source not found..**

Table 20 Standard Boot Sequence

Parameter	Min	Typ	Max	Units	Comments
<code>tboot_delay</code>			6	s	The time between mote power up and serial interface availability.

7.6.2 Low Current Boot

When operating in Low Current Boot, the DN2510 lowers average current consumption by spreading the boot operation over a longer time. This mode is intended to support systems with supplies having a maximum DC current less than the peak current required by the DN2510. These systems must store enough charge to maintain the supply through the DN2510's peak current consumption. The peak "average current" consumption for the M2510 is defined by the maximum total charge Q consumed over a sliding window in time, T_{window} .

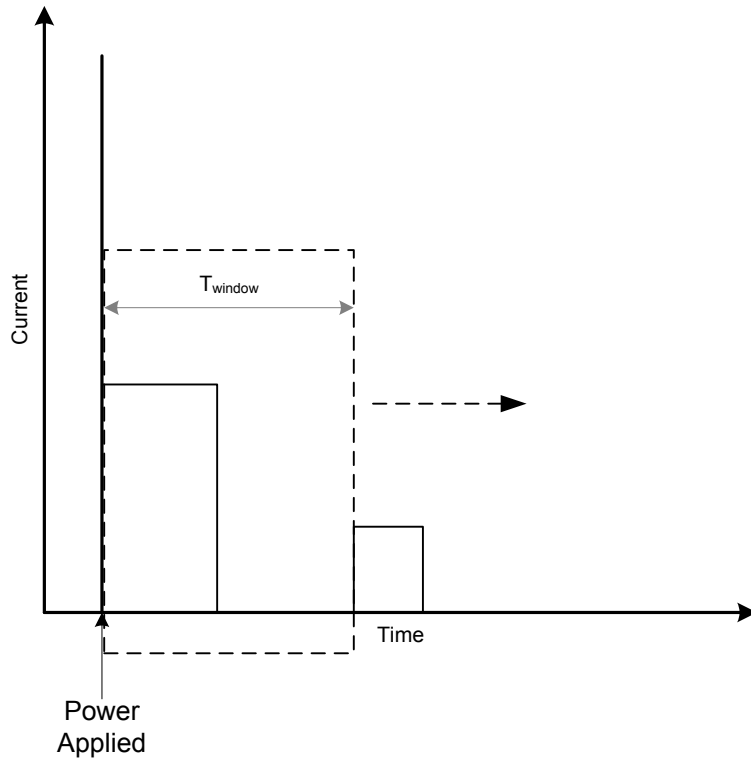


Figure 12 Low Current Boot Sequence

Table 21 Low Current Boot Sequence

Parameter	Min	Typ	Max	Units	Comments
tboot_delay			TBD	s	The time between mote power up and serial interface availability.
Twindow			TBD	ms	
Q			2.5	mC	

Figure 13 " " for value of tboot_delay)

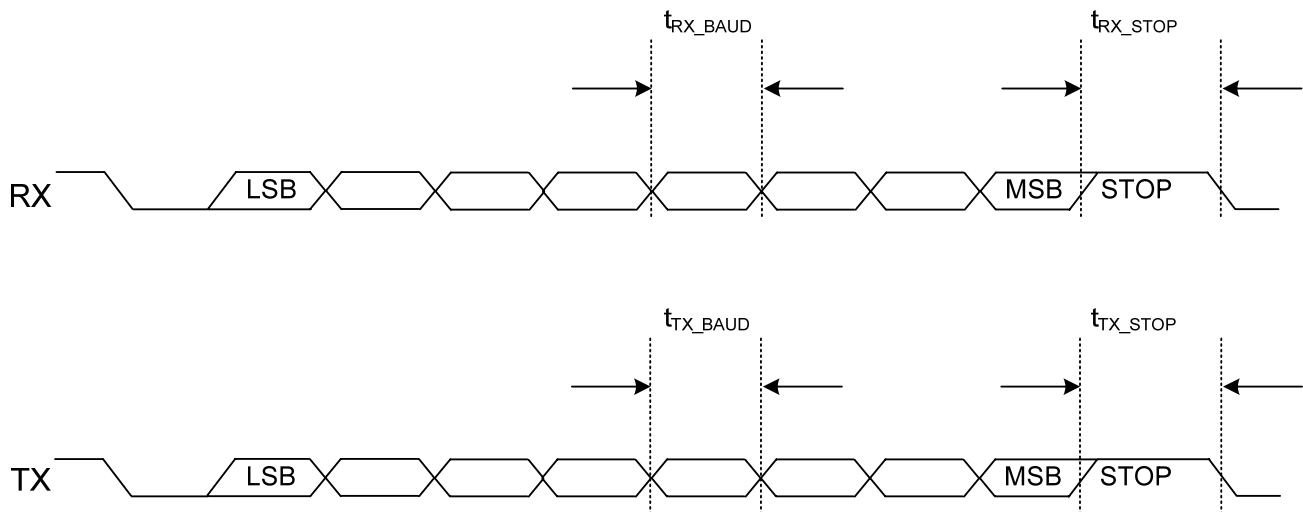


Figure 14 Byte-level Timing

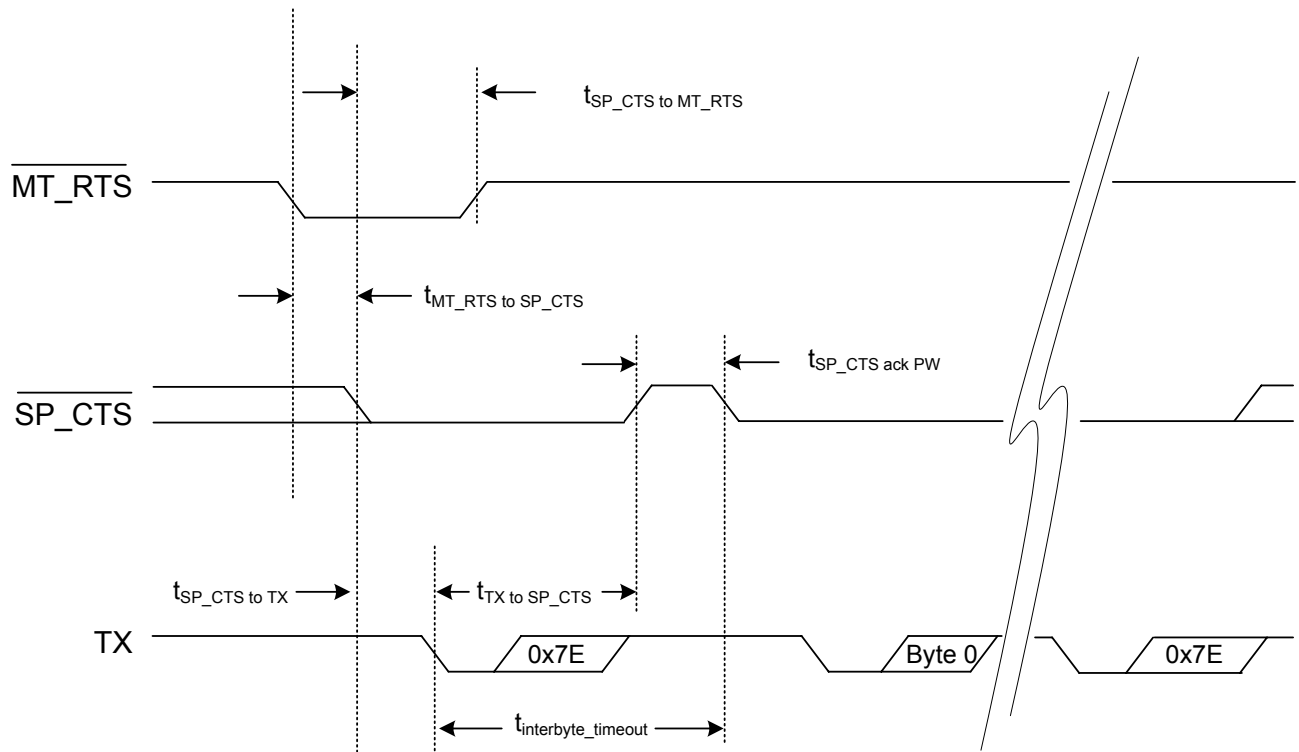


Figure 15 Flow Control Timing

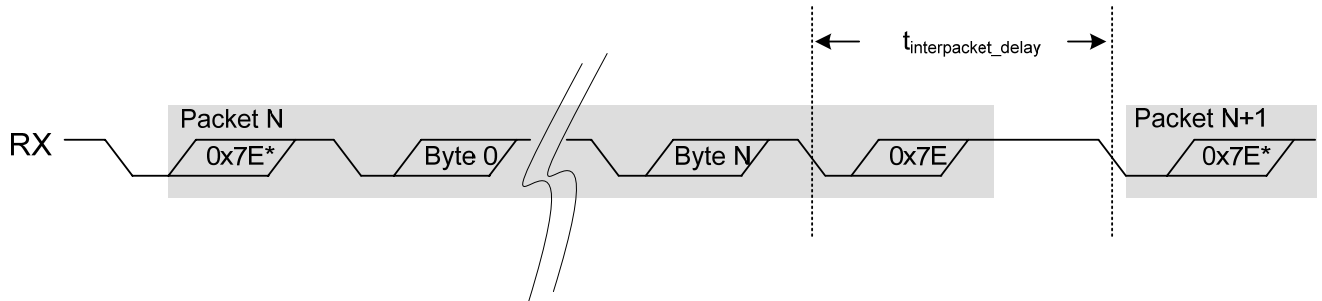


Figure 16 Packet Timing

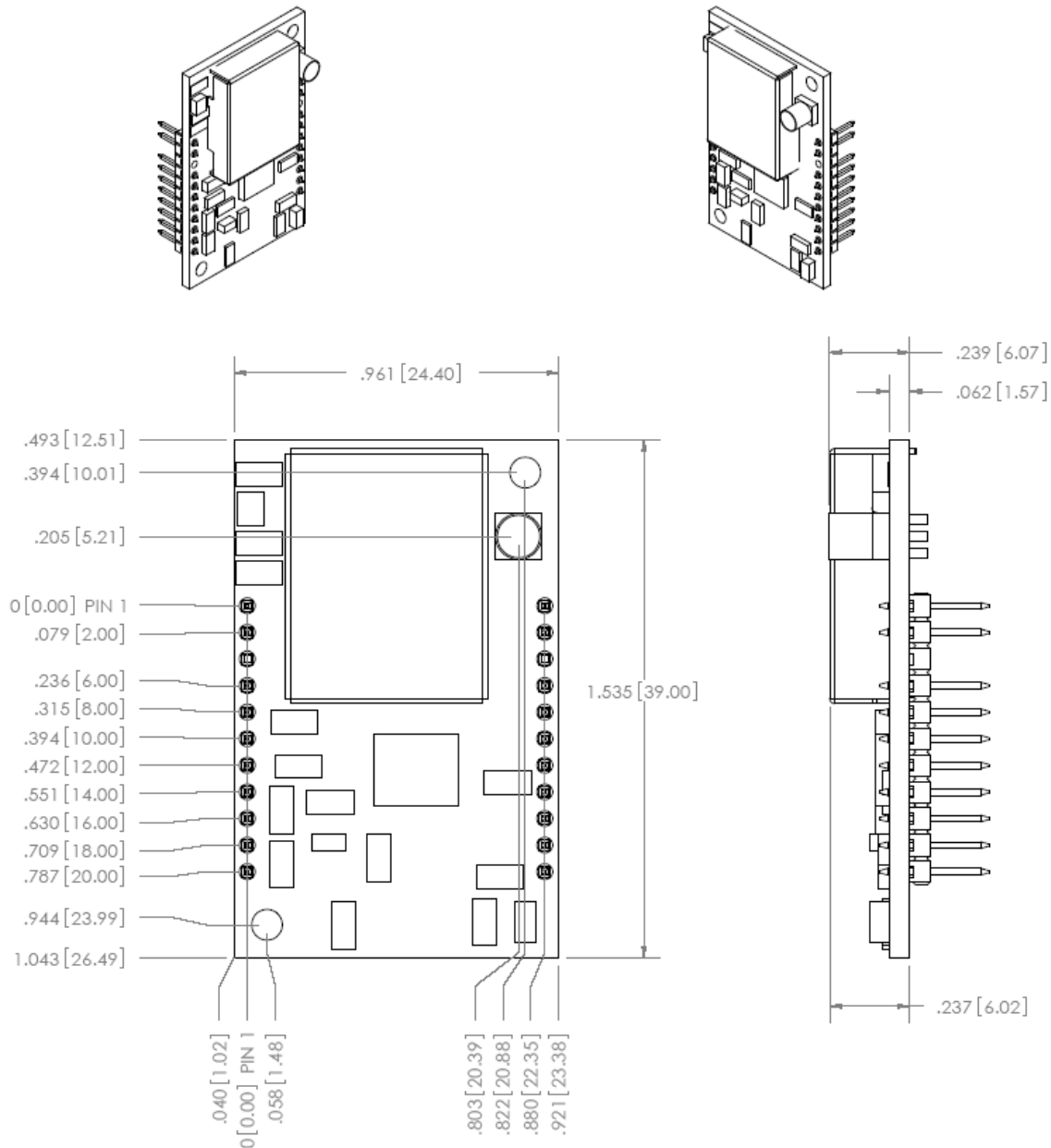
* For Mode 3 (115.2 kbps) the framing byte, 0x7E, must be repeated at the start of each packet set to the M2510.

7.7 Mote Serial API

The M2510 offers a comprehensive application programming interface (API) that provides full programmatic access to control the mote, monitor its status, and for access to the wireless mesh network. Please refer to the *SmartMesh IA-510 Mote Serial API Guide* for more information.

8.0 Packaging Description

8.1 Mechanical Drawing



600-0101 REV 2

PRIMARY DIMENSIONS ARE IN INCHES.
DIMENSIONS IN [mm] ARE MILLIMETERS

Figure 17 M2510 Mote Mechanical Drawing

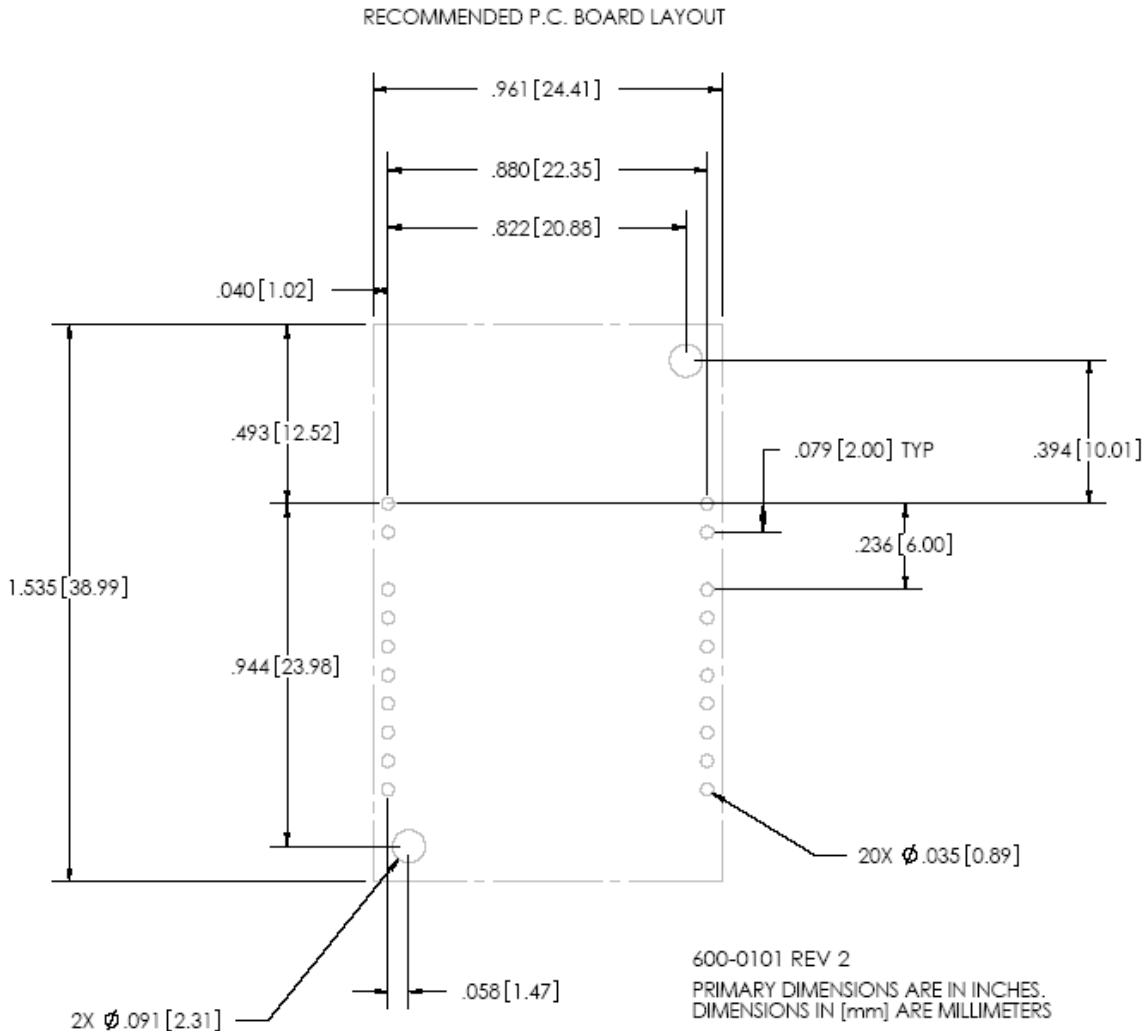


Figure 18 M2510 Mote Footprint

8.2 Soldering Information

The M2510 can be hand soldered with a soldering iron at 230 °C. The soldering iron should be in contact with the pin for 10 seconds or less.

9.0 Regulatory and Standards Compliance

9.1 FCC Compliance

9.1.1 FCC Testing

The M2510 mote will comply with Part 15.247 modular (Intentional Radiator) of the FCC rules and regulations. In order to fulfill FCC certification requirements, products incorporating the M2510 mote must comply with the following:

1. An external label must be provided on the outside of the final product enclosure specifying the FCC identifier as described in 9.1.3 below.
2. The antenna must be electrically identical to the FCC-approved antenna specifications for the M2510 as described in 9.1.2, with the exception that the gain may be lower than specified in Table 22.
3. The device integrating the M2510 mote may not cause harmful interference and must accept any interference received, including interference that may cause undesired operation.
4. An unintentional radiator scan must be performed on the device integrating the M2510 mote, per FCC rules and regulations, CFR Title 47, Part 15, Subpart B. See FCC rules for specifics on requirements for declaration of conformity.

9.1.2 FCC-approved Antennae

The following are FCC-approved antenna specifications for the M2510

Table 22 FCC-approved Antenna Specifications for the M2510

Gain	Pattern	Polarization	Frequency	Connector
+2 dBi maximum	Omni-directional	Vertical	2.4-2.4835 GHz	MMCX

9.1.3 OEM Labeling Requirements

The Original Equipment Manufacturer (OEM) must ensure that FCC labeling requirements are met. The outside of the final product enclosure must have a label with the following (or similar) text specifying the FCC identifier. The FCC ID and certification code must be in Latin letters and Arabic numbers and visible without magnification.

Contains transmitter module FCC ID: *SJC-M2140*

Or

Contains FCC ID: *SJC-M2140*

9.2 Industry Canada (IC) Compliance

9.2.1 IC Testing

The M2510 will be certified for modular Industry Canada (IC) RSS-210 approval. The OEM is responsible for its product to comply with IC ICES-003 and FCC Part 15, Sub. B - Unintentional Radiators. The requirements of ICES-003 are equivalent to FCC Part 15 Sub. B and Industry Canada accepts FCC test reports or CISPR 22 test reports for compliance with ICES-003.

9.2.2 IC-approved Antennae

The M2510 is designed to operate with the antennas meeting the maximum gain and specifications shown in Table 23. Antennas not meeting the specifications in Table 23 are strictly prohibited for use with this device. The required antenna impedance is 50 Ohms. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Table 23 IC-approved Antenna Specifications for the M2510

Gain	Pattern	Polarization	Frequency	Connector
+2 dBi maximum	Omni-directional	Vertical	2.4-2.4835 GHz	MMCX

9.2.3 OEM Labeling Requirements

The Original Equipment Manufacturer (OEM) must ensure that IC labeling requirements are met. The outside of the final product enclosure must have a label with the following (or similar) text specifying the IC identifier. The IC ID and certification code must be in Latin letters and Arabic numbers and visible without magnification

Contains IC: *5853-M2140*

9.3 CE Compliance

9.3.1 Declaration of Conformity

Product declaration pending formal product evaluation.

SmartMesh IA-510 M2510 shall be evaluated against the appropriate standards ETSI EN 300 328, ETSI EN 301 489-17 and EN 60950, following the provisions of Radio Equipment and Telecommunication Terminal Equipment directive 99/5/EC with requirements covering EMC directive 89/336/EEC, and Low voltage directive 73/23/EEC.

9.3.2 European Compliance

If the M2510 mote is incorporated into a product, the manufacturer must ensure compliance of the final product to the European harmonized EMC and low-voltage/safety standards. A Declaration of Conformity must be issued for each of these standards and kept on file as described in Annex II of the R&TTE Directive. Furthermore, the manufacturer must maintain a copy of this M2510 user documentation and ensure the final product does not exceed the specified power ratings, antenna specifications, and/or installation requirements as specified in the user manual. If any of these specifications are exceeded in the final product, a submission must be made to a notified body for compliance testing to all required standards.

9.3.3 OEM Labeling Requirements

The ‘CE’ marking must be affixed to a visible location on the OEM product. The CE mark shall consist of the initials “CE” taking the following form:

If the CE marking is reduced or enlarged, the proportions given in the drawing below must be respected.

The CE marking must have a height of at least 5 mm except where this is not possible on account of the nature of the apparatus.

The CE marking must be affixed visibly, legibly, and indelibly.

Furthermore, since the usage of the 2400 – 2483.5 MHz band is not harmonized throughout Europe, the Restriction sign must be placed to the right of the ‘CE’ marking as shown below. See the R&TTE Directive, Article 12 and Annex VII for more information.

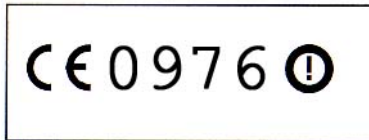


Figure 19 CE Label Requirements

9.3.4 Restrictions

Norway—Norway prohibits operation near Ny-Alesund in Svalbard. More information can be found at the Norway Posts and Telecommunications site (www.npt.no).

9.4 Compliance to Restriction of Hazardous Substances (RoHS)

Restriction of Hazardous Substances (RoHS) is a directive that places maximum concentration limits on the use of cadmium (Cd), lead (Pb), hexavalent chromium (Cr+6), mercury (Hg), Polybrominated Biphenyl (PBB) and Polybrominated Diphenyl Ethers (PBDE). Dust Networks is committed to meeting the requirements of the European Community directive 2002/95/EC.

This product has been specifically designed to utilize RoHS compliant materials and to eliminate, or reduce, the use of restricted materials to comply with 2002/95/EC.

The Dust Networks RoHS compliant design features include:

- RoHS compliant solder for solder joints
- RoHS compliant base metal alloys
- RoHS compliant precious metal plating
- RoHS compliant cable assemblies and connector choices

NOTE: In accordance with compliance to 2002/95/EC, Dust Network customers will elect to use certain types of lead-free solder alloys. A corresponding change in process as to optimum reflow temperatures will be required, and must be carefully evaluated.

9.5 Industrial Environment Operation

The M2510 is designed to meet the specifications of a harsh industrial environments which includes:

- **Shock and Vibration**—The M2510 complies with high vibration pipeline testing, as specified in IEC 60770-1.
- **Temperature Extremes**—The M2510 is designed for industrial storage and operational temperature range of –40 °C to +85 °C.

10.0 Related Documentation

- *SmartMesh IA-510 DN2510, M2510 Integration Guide*
- *SmartMesh IA-510 Mote Serial API Guide*

11.0 Ordering Information

Product List:

M2510: SmartMesh IA-510 2.4 GHz Mote

Contact Information:

Dust Networks

30695 Huntwood Ave.

Hayward, CA 94544

Toll-Free Phone: 1 (866) 289-3878

Website: www.dustnetworks.com

Email: sales@dustnetworks.com

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Last Revised: February 15, 2008

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Advanced Information	Planned or under development	This datasheet contains the design specifications for product development. Dust Networks reserves the right to change specifications in any manner without notice.
Preliminary	Engineering samples and pre-production prototypes	This datasheet contains preliminary data; supplementary data will be published at a later time. Dust Networks reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. The product is not fully qualified at this point.
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